Novel Technique for Reducing the Comparator Delay Dispersion in 45nm CMOS Technology for Level-Crossing ADCs

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Abstract:

This paper demonstrates a new technique to reduce the comparator delay dispersion caused by variable input overdrive. In the proposed technique, the conventional comparator circuit is modified by adding a variable driving-current block (VDCB) which is used such that it supplies the output node of the differential amplifier with a current that is inversely proportional with the level of input signal. Therefore the overdrive- caused delay dispersion is effectively reduced. The technique incurs small area overhead (only three transistors) compared with the previous works. The proposed circuit is implemented in 45nm technology. The effect of process variation on the performance of the proposed technique is studied by simulation. The results show that the overdrive-related propagation delay dispersion of the proposed technique is 26% of its counterpart in the conventional comparator for an input frequency up to 500MHz. The power consumption is 220 W at 200MHz.

Keywords:

Comparator , Levelcrossing ADCs , Propagation delay dispersion

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