Assiut university
Staff Researches

CMOS Flash TDC with 0.84 ~ 1.3 ps Resolution Using Standard Cells

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Abstract:

This paper proposes a new flash time-to-digital converter (TDC) design, which incorporates deterministic, variable delay into the decision elements. These are implemented with cross-coupled NAND standard cells of variable transistor widths. Both experiment and simulation are used to validate this new design, which provides variable time-difference ranges by controlling the input slew rate. It is also possible to use the proposed flash TDC as a soft macro.

Keywords:

arbiter , deterministic variable delay , flash TDC , slope control

Published In:

RFIC 2012, Montreal- Canada , ,