10 Gbit/s 2mW Inductorless Transimpedance Amplifier

M. Atef and H. Zimmermann

Abstract:

This work presents the design and performance of a 10Gbit/s transimpedance amplifier (TIA) implemented in a 40nm CMOS technology. The introduced TIA uses an inverter with active common-drain feedback (ICDF-TIA). The TIA is followed by a two-stage differential amplifier and a 50Ω differential output driver to provide an interface to the measurement setup. The optical receiver shows an optical sensitivity of −19dBm for a BER= 10−12. The transimpedance amplifier achieves a transimpedance gain of 47dBΩ, 8GHz bandwidth with 0.45pF total input capacitance for the photodiode, ESD protection and input PAD. The TIA occupies 0.0002mm2 whereas the complete optical receiver occupies a chip area of 0.16mm2. The power consumption of the TIA is only 2mW and the complete chip dissipates 16mW for a 1.1V single supply voltage. The complete optical receiver has a 58dBΩ transimpedance gain and 7GHz bandwidth.

Keywords:

Bandwidth;CMOS integrated circuits;Impedance;Inverters;Noise;Optical receivers;Power demand

Published In:

IEEE International Symposium on Circuits and Systems (ISCAS2012), Seoul, South Korea , , pp. 1728 -1731