8 Gbits/s inductorless transimpedance amplifier in 90 nm CMOS technology

Mohamed Atef, Francisco Aznar, Stefan Schidl, Andreas Polzer, Wolfgang Gaberl, Horst Zimmermann

Abstract:

This work presents the design and the measured performance of a 8 Gb/s transimpedance amplifier (TIA) fabricated in a 90 nm CMOS technology. The introduced TIA uses an inverter input stage followed by two common-source stages with a 1.5 k feedback resistor. The TIA is followed by a single-ended to differential converter stage, a differential amplifier and a 50 differential output driver to provide an interface to the measurement setup. The optical receiver shows a measured optical sensitivity of 18.3 dBm for a bit error rate = 109. A gain control circuitry is integrated with the TIA to increase its input photo-current dynamic range (DR) to 32 dB. The TIA has an input photo-current range from 12 to 500 A without overloading. The stability is guaranteed over the whole DR. The optical receiver achieves a transimpedance gain of 72 dB and 6 GHz bandwidth with 0.3 pF total input capacitance for the photodiode and input PAD. The TIA occupies 0.0036 mm2 whereas the complete optical receiver occupies a chip area of 0.46 mm2. The power consumption of the TIA is only 12 mW from a 1.2 V single supply voltage. The complete chip dissipates 60 mW where a 1.6 V supply is used for the output stages.

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