



(1)

Optical NoC Design-Parameters Exploration and Analysis

Atef Allam Ian O'Connor

Abstract:

Abstract—Optical network-on-chip (ONoC) is a well accepted emerging technology for use as a communication platform for system-on-chip (SoC). Due to its heterogeneous nature, tools for its design and analysis have become a necessity. In this paper, we present a tool for the exploration and validation of ONoC building block design parameters. The proposed methodology explores and verifies the joint feasibility of optoelectronic and photonic devices specifications for successful and reliable data communication. This is achieved through building a library of matching and chainable sets of optoelectronic and photonic devices. This library can be used for ONoC system-level design and analysis as well as during the design phase of these devices.

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(2)

Optical Network-on-Chip Reconfigurable Model for Multi-Level Analysis

Atef Allam Ian O'Connor Alberto Scundurra

Abstract:

Abstract Optical network-on-chip (ONoC) is a well accepted emerging technology for use as a communication platform for systems-on-chip (SoC). Its heterogeneous nature dictates developing a hierarchical model and tools for its design and analysis. This paper presents a reconfigurable ONoC model that can be used for analyzing the network at three hierarchical levels: system level, behavioral level, and physical level. At system level, the proposed ONoC model can be used to evaluate the network performance metrics (e.g. latency and throughput). At behavioral level, the model can be used to analyze the functionality of the whole ONoC from the interaction and the integration of its constituent building blocks. At the physical level, the model can be used to analyze the effect and verify the joint feasibility of optoelectronic and photonic devices specifications for reliable data communication and can further be used as a reference golden model during the design phase of the physical devices. The proposed model has been integrated successfully inside an industrial simulation environment (ST GenKit) using an industrial standard (VSTNoC) protocol.

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(3)

-Performance Evaluation for Passive-Type Optical Network-on Chip

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Abstract:

Abstract Optical networks-on-chip (ONoCs) represent an emerging technology for use as a communication platform for systems-on-chip (SoC). It is a novel on-chip communication system where information is transmitted in the form of light, as opposed to the conventional electrical network-on-chip (ENoC). This work studies the performance of a class of ONoCs that employ a single central passive-type optical router using wavelength division multiplexing (WDM) as a routing mechanism. The ONoC performance analysis has been carried out both at system-level (network latency and throughput) and at the physical level. In physical-level (optical) performance analysis of the ONoC, we study the communication reliability of the ONoC formulated by the signal-to-noise ratio (SNR) and the bit error rate (BER). Optical performance of the ONoC is carried out based on the system parameters, component characteristics and technology. The system-level analysis is carried out through simulation using flit-level-accurate SystemC model. Experimental results prove the scalability of the ONoC and demonstrate that the ONoC is able to deliver a comparable bandwidth or even better (in large network sizes) to the ENoC.

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(4)

A Protocol Stack Architecture for Optical Network-on-Chip

Atef Allam Ian O'Connor

Abstract:

Abstract—As the Optical Network-on-Chip (ONoC) becomes a candidate solution for the communication infrastructure of the Systems-on-Chip (SoC), the development of proper hierarchical models and tools for its design and analysis, specific to its heterogeneous nature, becomes a necessity. This work presents a novel protocol stack architecture for the ONoC. The proposed protocol stack is a 4-layered hardware stack consisting of the physical layer, the physical-adapter layer, the data link layer, and the network layer. It allows the modular design of each ONoC building block that boosts the interoperability and design reuse of the ONoC. Using this protocol stack architecture, this paper also introduces the micro-architecture of a new router called Electrical Distributed Router (EDR) as a wrapper for the ONoC. The proposed protocol stack has been modeled and integrated inside an industrial simulation environment (ST OCCS GenKit) using an industrial standard (VSTNoC) protocol.

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(5)

Memory Minimization for Tensor Contractions using Integer Linear Programming

Atef Allam, J. Ramanujam, G. Baumgartner, and P. Sadayappan

Abstract:

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(6)

Simultaneous Peak and Average Power Optimization in Synchronous Sequential Designs Using Retiming and Multiple Supply Voltages

Atef Allam and J. Ramanujam

Abstract:

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Keywords:

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(7)

Modified Force Directed Scheduling for Peak and Average Power Optimization Using Multiple Supply Voltages

Atef Allam and J. Ramanujam

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(8)

Dynamic Memory Usage Optimization using ILP

Atef Allam and J. Ramanujam

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(9)

ILP and Iterative LP Solutions for Peak and Average Power Optimization in HLS

Atef Allam and J. Ramanujam

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(10)

A Protocol Stack Architecture for Optical Network-on-Chip: Organization and Performance Evaluation

Atef Allam and Ian O'Connor

Abstract:

Abstract Optical networks-on-chip (ONoCs) represent an emerging technology for use as a communication platform for systems-on-chip (SoC). It is a novel on-chip communication system where information is transmitted in the form of light, as opposed to conventional electrical networks-on-chip (ENoC). As the ONoC becomes a candidate solution for the communication infrastructure of the SoC, the development of proper hierarchical models and tools for its design and analysis, specific to its heterogeneous nature, becomes a necessity. This chapter studies a class of ONoCs that employ a single central passive-type optical router using wavelength division multiplexing (WDM) as a routing mechanism. A novel protocol stack architecture for the ONoC is presented. The proposed protocol stack is a 4-layered hardware stack consisting of the physical layer, the physical-adaptor layer, the data link layer, and the network layer. It allows the modular design of each ONoC building block, thus boosting the interoperability and design reuse of the ONoC. Adapting this protocol stack architecture, this chapter introduces the micro-architecture of a new router called electrical distributed router (EDR) as a wrapper for the ONoC. Then, the performance of the ONoC layered architecture has been evaluated both at system-level (network latency and throughput) and at the physical (optical) level. Experimental results prove the scalability of the ONoC and demonstrate that the ONoC is able to deliver a comparable bandwidth or even better (in large network sizes) to the ENoC. The proposed protocol stack has been modeled and integrated inside an industrial simulation environment (ST OCCS GenKit) using an industrial standard (VSTNoC) protocol.

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(11)

Power and memory optimization techniques in embedded systems design

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