An Ultralow-Power High-Gain Biopotential Amplifier for Electromyogram Signal Recording

Ehab A. Hamed[1], Mohamed Atef[1] and Mohamed Abbas[1,2]
[1]Department of Electrical Engineering, Faculty of Engineering, Assiut University Assiut 71512, Egypt
[2]Electrical Engineering Department, College of Engineering, King Saud University, Kingdom of Saudi Arabia
ehab_ali@eng.au.edu.eg; moh_atef@aun.edu.eg; m-abbas@aun.edu.eg

***Abstract*—This paper introduces a design for an ultralow-power electromyogram (EMG) signal amplifier with low noise operation. The design consists of two stages, the first stage is highly efficient but supply-sensitive single ended amplifier and the second stage is differential, to improve the supply rejection ratio and common mode rejection ratio. Each stage is configured with cascode MOSFET transistors to increase the gain value. The proposed design is simulated by 130 nm CMOS, and its results are reported. The design achieves 60.62 dB mid-band gain with bandwidth of 1.72kHz. Using a supply voltage of 1.1 V, the amplifier consumes 1.03 µA of current. Input referred noise is 3.006 μV_{rms}. The common mode and power supply rejection ratios are above 49.05 dB and 55.72 dB respectively.**

Keywords— Electromyogram, EMG, power supply rejection ratio (PSRR), Common mode rejection ratio (CMRR), ultralow power, current-reuse complimentary input (CRCI).

I. INTRODUCTION

EMG signal is small electrical currents generated by muscle fibers prior to the production of muscle force [1]. It has been increasingly used in the study of muscular activities including assessment, treatment planning, evaluation of progress and outcomes, rehabilitation, worksite ergonomic design, sports training, and research [2], [3].

In prior work, a system for transferring EMG signal between Limbs, to train the limb muscles that suffers from peripheral nerve injury, was introduced. The system was consisting form sensing circuit, control unit and stimulating circuit [4]. The amplifier in the sensing circuit was AD620 instrumentation amplifier, which has relatively high-power dissipation [5].

Over the past several years there has been numerous number of researches for designing low-power bio-medical signal amplifiers. The capacitive feedback approach is the most popular topology. It uses capacitors to make the midband gain equals the input capacitance divided by the feedback capacitance (Ci/Cf) and ensures dc offset rejection [6]. Extremely low power dissipation can be achieved by using open-loop single-ended current-reuse complimentary input (CRCI) amplifier in trade off poor linearity and low power supply rejection ratio (PSRR) [7]. Most of amplifier designs till now are optimized for general bio-medical signals as the electroencephalography (EEG), the electromyogram (EMG), the electrocardiogram (ECG), and the electrooculography (EOG), which makes them obliged to cover wide bandwidth (BW) of frequencies. Considering one type of bio-medical signals helps to reach the optimum design for it.

The proposed design is optimized for EMG signal characteristics which has a typical passband frequency ranges from between 10Hz (high pass filtering) to 1000Hz (low-pass filtering) [1], [8]. Using cascode MOSFETs in the output of each stage helped on getting higher gain within this range of bandwidths. EMG signal requires high common mode rejection ratio (CMRR), which is reached by using differential OTA, and using cascode MOSFET with the current mirror of the second stage to increase current mirror's output resistance.

The rest of the paper is organized as follows. Section II presents the design architecture of the EMG signal amplifier. Simulation results are shown in Section III. followed by the conclusion in Section IV.

II. EMG SIGNAL AMPLIFIER ARCHITECTURE

The proposed EMG amplifier, shown in Fig. 1, has two stages working from 1.1V voltage supply source. The first stage consists of two identical single ended amplifiers with capacitive feedback and current-reuse complimentary-input (CRCI), each one, by itself, gives extremely low power dissipation but poor PSRR. The second stage is a fully differential OTA with capacitive feedback. The symmetric supply noise at the outputs of the first stage branches is suppressed as a common-mode signal by the second stage, so the full amplifier achieves high PSRR [6], [9].

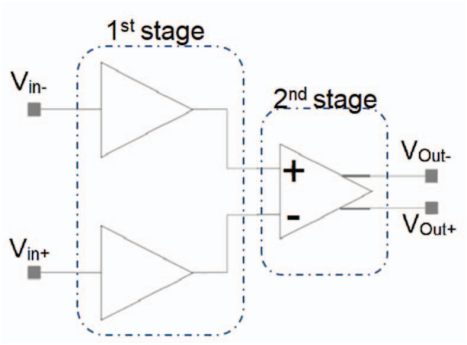


Fig. 1. EMG signal ampilifier configuration

A. First Stage Design

First stage single ended schematic is shown in Fig. 2(a). AC coupling is implemented using MOS-bipolar pseudo-resistors (PR) in conjunction with on chip capacitor (C1) to reject large DC offsets of the electrodes [7], [9]. The topology of the pseudo-resistors (PR) in Fig. 2(b) is characterized by a very high impedance. Under 0.13 µm CMOS process, conventional nominal-threshold pseudo resistors are insufficient due to the increasing leakage current so using thick-oxide PMOS transistors is needed [10]. Same pseudo-resistors are used also in the second stage. Capacitive feedback in first stage is used to enhance gain accuracy and linearity giving midband gain equals C1/Cf1 [9].

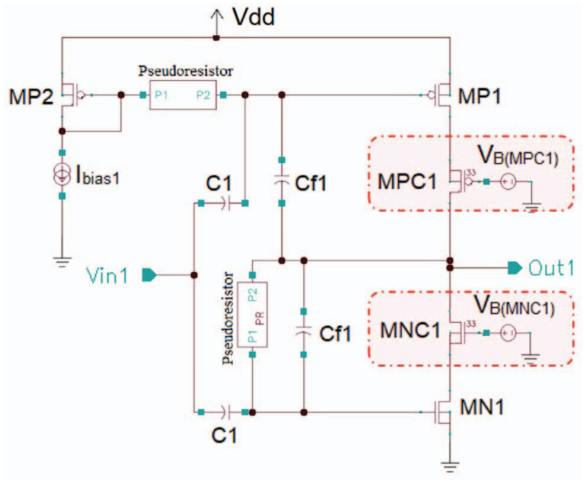


Fig. 2. (a) Schematic of the first-stage amplifier. (b) Pesudoresistors used in first and second stages.

The bias current (I_{bias1} = 40nA) is quarter the input transistors current, so it has a little contribution in the total current of the first stage. The RC network, used in MP1 AC coupling, presents a low-pass filter to the diode connected transistor MP2, helping in suppress the noise from the current source.

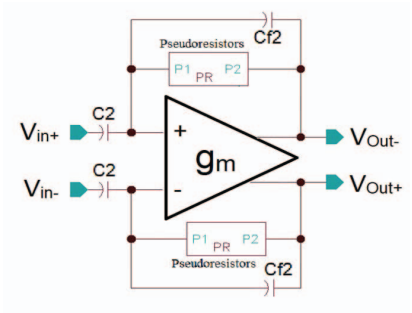
The amplifier transconductance is doubled by driving the gates of both MP1 and MN1, as their gates are DC decoupled through the AC coupling capacitors. Since the output noise is still the same, the input-referred noise voltage is divided by two [7], [9]. Adding cascode thick-oxide MOSFET transistors MPC1 and MNC1 to the output of the first stage helps in getting high gain and reducing bandwidth to fit the EMG frequencies range by increasing the output resistance of the amplifier.

B. Second Stage Design

The second stage fully differential capacitive feedback amplifier schematic is shown in Fig. 3(a). As in the first stage, the midband gain of this stage is determined by the capacitors ratio C2/Cf2. Similar pesudoresistors topology and W/L ratios of first stage is used in the second one. Cascode thick-oxide MOSFET transistors MPC7, MPC8, MNC4 and MNC5 are added to the output of the second stage for the same purpose as it for the first stage.

Current mirror OTA of the second stage schematic is shown in Fig. 3(b). The current mirror ratio is 1:4, but the bias current Ibias2 = 100nA. Cascode MPC3 transistor is used for increasing the output resistance of the current mirror to achieve a good CMRR. Since the supply noise from the two channels of the first stages are identical, then increasing CMRR of the second stage leads obligatory to increase PSRR.

A Common mode feedback (CMFB) is used to stabilize the common mode voltage by taking the average voltage of the differential outputs and inject it to the gate of MP7 and MP8.



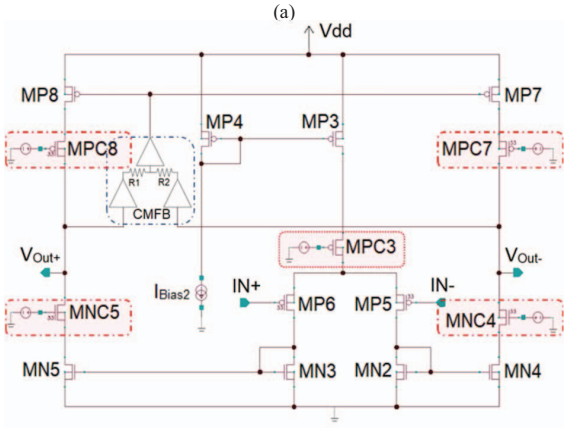


Fig. 3. (a) Schematic of the second-stage amplifier. (b) Schematic of the OTA.

C. Equivalent circuit for biopotential electrode

For purpose of simulation, the equivalent circuit for biopotential electrode, shown in Fig. 4, is added after the input signal source and before the first stage amplifier. Rs is the series resistance associated with interface effects and the resistance of the electrode materials themselves. Rd and Cd represent the impedance associated with the electrode-electrolyte interface

and polarization effects. The battery Vhc represents the half-cell potential [10], [11].

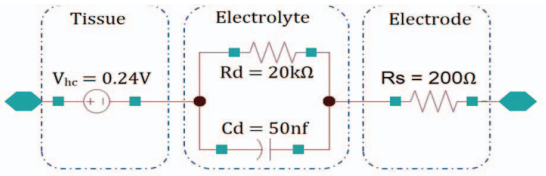


Fig. 4. Equivalent circuit for biopotential electrode.

D. *Parameters of the proposed amplifier*

Capacitors determine the midband gain of each stage. The input capacitance (C1) of first stage value is 130pf, while the feedback capacitance (Cf1) is 2pf. For the second stage, the input capacitance (C2) is 16pf, while the feedback capacitance (Cf2) is 0.8pf. Transistor sizing and biasing voltage is listed in Table I.

TABLE I. TRANSISTORS SIZING FOR THE PROPOSED AMPLIFIER

First Stage		
Transistor	***Sizing***	***Bias Voltage***
MPC1	10u/10u	0.1 V
MNC1	2u/10u	0.8 V
MP1	40u/10u	
MP2, MN1	10u/10u	
Second Stage		
Transistor	***Sizing***	***Bias Voltage***
MPC3	1u/11.6u	0.7 V
MPC7, MPC8	1u/10u	0.2 V
MNC4, MNC5	1u/25u	0.8 V
MP3	4u/2u	
MP4	1u/2u	
MP5, MP6	100u/2u	
MP7, MP8	0.8u/20u	
MN2, MN3, MN4, MN5	2u/20u	

III. RESULTS AND DISCUSSION

The proposed EMG amplifier is simulated in 130 nm CMOS technology using Cadence CAD tools. The full amplifier draws a current of 1.03 µA. Each branch of the first stage draws a current of 0.412 µA and the second stage draws 0.208 µA from 1.1 V supply. This makes the total power dissipation of the design is 1.133 µW, which is a very low power for an amplifier of two stages.

The frequency response of the amplifier is shown in Fig.5(a). Its midband gain is 60.52 dB (the first stage contributed in 36.01 dB and the second stage contributed in 24.86 dB). The 3dB bandwidth is from 1.2 Hz to 1.72 kHz, which is sufficient for EMG signal as mentioned in the introduction.

The input impedance (Zin) of the proposed amplifier is shown in Fig. 5(b), with maximum of 620 MΩ and minimum of 1.12 MΩ at the highest frequency. It is clear that the input stage impedance is several times higher than the electrode impedance, so most of acquired voltage will be collected and amplified by the input stage.

The integrated input referred noise is 3 µVrms in range between 1 Hz to 2kHz. The input referred noise spectrum is shown in Fig. 5(c). The lowest value of CMRR, in the passband range, is 49 dB, and it is mostly 49.91 dB as shown in Fig. 6. For PSRR the lowest value is 55.72 dB as shown in Fig. 6.

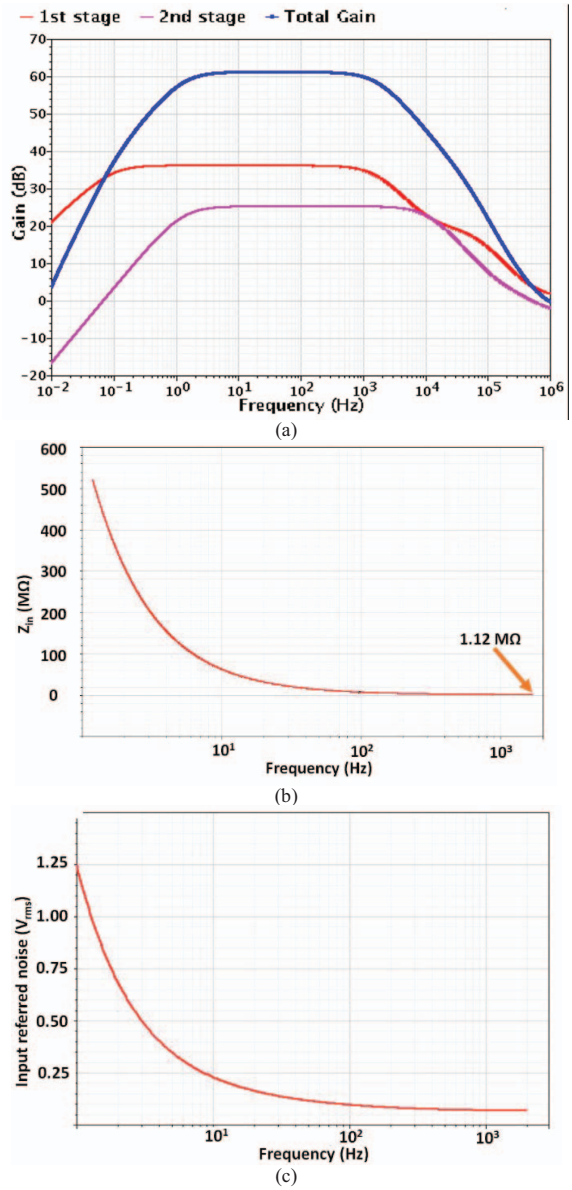


Fig. 5. (a) Frequency response of the first stage, second stage and full amplifier. (b) The input impedance (Zin). (b) Input-referred noise spectrum of the proposed amplifier.

The proposed amplifier is compared with other state of art bio-medical signal amplifiers in Table II. The comparison shows the power efficiency of the proposed design. The Noise efficiency factor (NEF) is calculated by (1) [6].

$$NEF = V_{in,rms}\sqrt{\frac{2I_{tot}}{\pi . U_T . 4kT . BW}} \qquad (1)$$

TABLE II. EMG AMPLIFIER PERFORMANCE COMPARISON WITH THE STATE OF ART BIO-AMPLIFIERS

	This work#	***This work# + [9] ****	***[6]***	***[7]***	***[9]***	***[12]***	***[13]***	
Supply voltage (V)	1.1	1.1	±2.5	1	1	1.8	2.5	
Supply current (µA)	1.03	1.4	16	0.805	2.85	6.1	3.6	0.32
Power dissipation (µW)	1.133	1.54	40	0.805	2.85	10.98	9	0.8
Gain (dB)	60.62	51.95	39.5	36.1	57.7	48/60	40.3	
Bandwidth (Hz)	1.2-1.72k	0.96-5.42k	0.025-7.2k	0.3-4.7k	0.49-10.5k	1-9k	10k	1k
Input referred noisre (μV_{rms})	3.006	3.147	2.2	3.6	3.04	3.5	2.81	
CMRR (dB)	> 49.05	> 58.6	> 83	-	> 45	48	82	
PSRR (dB)	> 55.72	> 65.35	> 85	5.5	> 50	55	82	
THD	3.7% @1mV_{PP}	0.052% @1mV_{PP}	1% @16.7mV_{PP}	7.1% @1mV_{PP}	1.6% @1mV_{PP}	1.2% @1mV_{PP}	0.1% @4.3mV_{rms}	0.1% @4.1mV_{rms}
Noise efficiency factor (NEF)	2.84	1.95	4.8	1.8	1.93	3.35	2.05	1.93
Figure of merit (FOM)	543	442.7	7.7	103.5	930	234.2	40.9	46
CMOS technology (µm)	130 nm	130 nm	1.5 µm	0.5 µm	90 nm	0.8 µm	0.35 µm	

*#Simulation. *The parameters of this work are applied to the work of [9] using 130 nm CMOS tech. without any cascode transistors.*

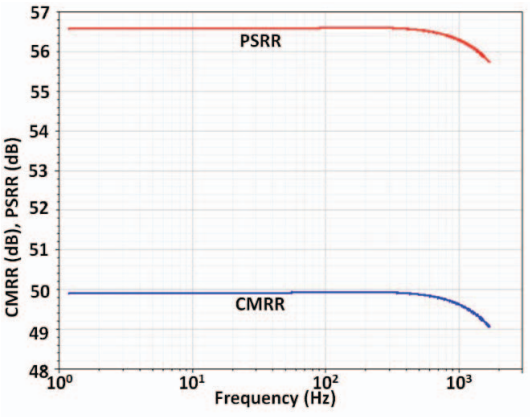


Fig. 6. CMRR and PSRR of the proposed design.

A figure of merit (FOM) has been added to the comparison. This FOM depends on input referred noise (Vin,rms), bandwidth (BW), power and midband gain(AVmid(asbs)) as in equation (2). The proposed amplifier shows the highest FOM between others, except for [9] whichhas higher FOM. Work in [9] uses smaller CMOS technology (90nm) which has higher unity gain bandwidth (ft) than (130nm), to get some fair comparison the same design parameters of the proposed design are used to simulate [9] and the results is added to the comparison in the second column showing the efficient of cascode topology in the FOM.

$$FOM = \frac{A_{Vmid}(abs) * BW(kHz)}{V_{in,rms}(\mu V) * Power(\mu W)} \qquad (2)$$

IV. CONCLUSION

This paper introduced an improved design of an EMG signal amplifier. The design adopted using cascode transistors, in the outputs of each stage, which helped in improving the midband gain of the amplifier and granted a suitable bandwidth for the EMG signal. Adding cascode transistor to the current mirror of the second stage increased its output resistance. The design was optimized to work for EMG signal, consuming extremely low power with low noise compared with the previous works.

References

[1] Scott Day. "Important factors in surface EMG measurement." Bortec Biomedical Ltd publishers, pp. 1-17, 2002.

[2] Igor Luiz Bernardes de Moura, Luan Carlos de Sena Monteiro Ozelim, and Fabiano Araujo Soares. "Low Cost Surface Electromyographic Signal Amplifier Based On Arduino Microcontroller." World Academy of Science, Engineering and Technology, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, vol. 8, no. 2, pp. 310-314, 2014.

[3] Jeffrey R Cram. Introduction to surface electromyography. Aspen Publishers, 1998.

[4] Ehab A. Hamed, Mohamed Atef, Mohamed Abbas, and R. R. Gharieb. "Transferring electromyogram signal between limbs." In Electronics, Communications and Computers (JEC-ECC), 2016 Fourth International Japan-Egypt Conference, pp. 123-126, 2016.

[5] Analog Devices. "AD620 Datasheet." Low cost, Low Power Instrumentation Amplifier, 1999.

[6] Reid R. Harrison, and Cameron Charles. "A low-power low-noise CMOS amplifier for neural recording applications." IEEE Journal of solid-state circuits, vol. 38, no. 6, pp. 958-965, 2003.

[7] Jeremy Holleman and Brian Otis. "A sub-microwatt low-noise amplifier for neural recording." Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE, pp. 3930-3933, Aug 2007.

[8] Edward A. Clancy. "Design of a High–Resolution Surface Electromyogram (EMG) Conditioning Circuit." Diss. Worcester Polytechnic Institute , Jan 2012.

[9] Tan Yang and Jeremy Holleman. "An ultralow-power low-noise CMOS biopotential amplifier for neural recording." IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 10, pp. 927-931, Oct 2015.

[10] Zhang Xiaoyang. "Ultra low power circuits for wearable biomedical sensors." (Doctoral dissertation), 2014.

[11] Joseph D. Bronzino. Biomedical engineering handbook. Vol. 2. CRC press, Dec 1999.

[12] Piotr Kmon, and P. Gryboś. "Energy efficient low-noise multichannel neural amplifier in submicron CMOS process." IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 7, pp. 1764-1775, Jul 2013.

[13] Tzu-Yun Wang, Li-Han Liu, and Sheng-Yu Peng. "A power-efficient highly linear reconfigurable biopotential sensing amplifier using gate-balanced pseudoresistors." IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 2, pp. 199-203, Feb 2015.