Assiut University
Faculty of Engineering

EE0614-DIGITAL DESIGN
2nd Term Final Examination
2014/2015

Mechatronics Program
Time: 3 Hours

الامتحان مكون من أربع صفحات، الإجابة فى نفس ورقة الأسئلة.
حاول فى كل الأسئلة، النهاية العظمى ٤٠ درجة.
الإجابة النهائية يجب أن تكون مكتوبة فى المكان المخصص لها.

Question # 1: (4 Points)

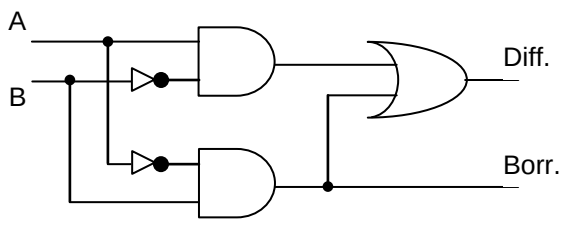
Consider the design of a circuit to subtract two binary bits, yielding a one- bit difference and a one-bit borrow. Four cases can arise:
0 from 0 result is 0 borrow 0, 0 from 1 result is 1 borrow 0, 1 from 0 result is 1 borrow 1, and 1 from 1 result is 0 borrow 0.
Using simple logic gates (AND, OR, Inverter) design a circuit that behaves in this way.

Dec.	Input		Output	
	A	B	Diff.	Borr.
0	0	0	0	0
1	0	1	1	1
2	1	0	1	0
3	1	1	0	0

Diff. = A.B' + A'.B

Borr. = A'.B

The Subtractor Logic Diagram



Question # 2: (3 Points)

The state of a 12-bit register is 100101010100. What is its content if it represents:
(a) Three decimal digits in BCD, (b) Three decimal digits in the excess-3 code,
(c) Three decimal digits in the 84-2-1 code?

BCD: 954

excess-3: 621

84-2-1: 734

Question # 3: (4 Points)

Using DeMorgan's theorem find the complement of the following expressions:

$F_1 = x'y' + x'z + y'z$
$F_2 = (A'B + CD')E + E'$

$$F_1' = (x + y)(x + z')(y + z')$$
$$= xy + xz' + yz'$$

$$F_2' = ((A + B')(C' + D) + E').E$$
$$= AC'E + ADE + B'C'E + B'DE$$

Question # 4: (4 Points)

A combinational circuit is defined by the following two Boolean functions:

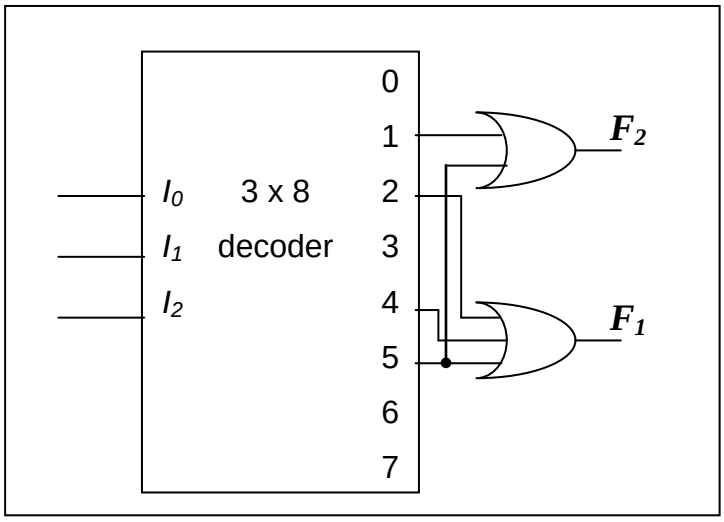
$F_1(x, y, z) = x'y\,z' + xy'$

$F_2(x, y, z) = y'z\,(x'z + xy')$

Find the min-terms of the functions, and implement them with a single decoder and external gates.

$F_1(x, y, z) = \Sigma m(2, 4, 5)$

$F_2(x, y, z) = \Sigma m(1, 5)$



Question # 5: (4 Points)

Derive the state table and the state diagram of the sequential circuit shown in Fig.5.

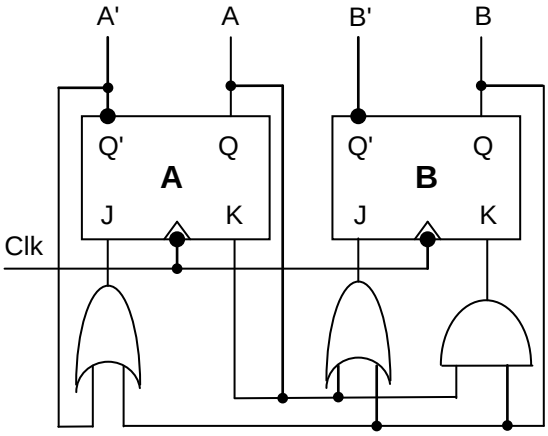
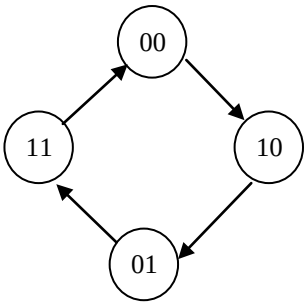


Fig.5

Present State		F.F. Inputs				Next State	
A	B	JA	KA	JB	KB	A	B
0	0	1	0	0	0	1	0
0	1	1	0	1	0	1	1
1	0	0	1	1	0	0	1
1	1	1	1	1	1	0	0



Question # 6: (3 Points)

Specify the number of address lines, data lines and the capacity in kilo-bytes of a 65536x32 RAM.

Address lines = 16 Lines

Data lines = 32 Lines

Capacity in Kbytes = 256 KB

Question # 7: (4 Points)

Show the main difference between latches and flip-flops by drawing the timing diagram of the output Q when applying the clk and input D shown in Fig. 7 to:

i) A positive level-triggered latch,
ii) A negative edge-triggered flip-flop.

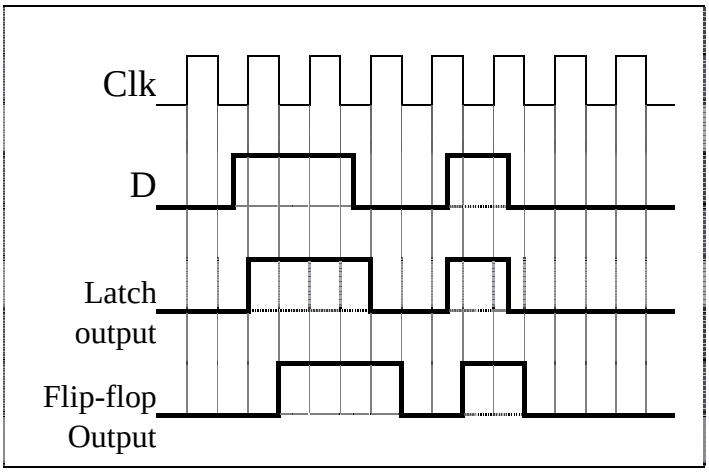


Fig. 7

Question # 8: (6 Points)

Design a synchronous mod-6 counter (counts 0-5) using T flip-flops and logic circuitry. Consider the unused states as don't care.

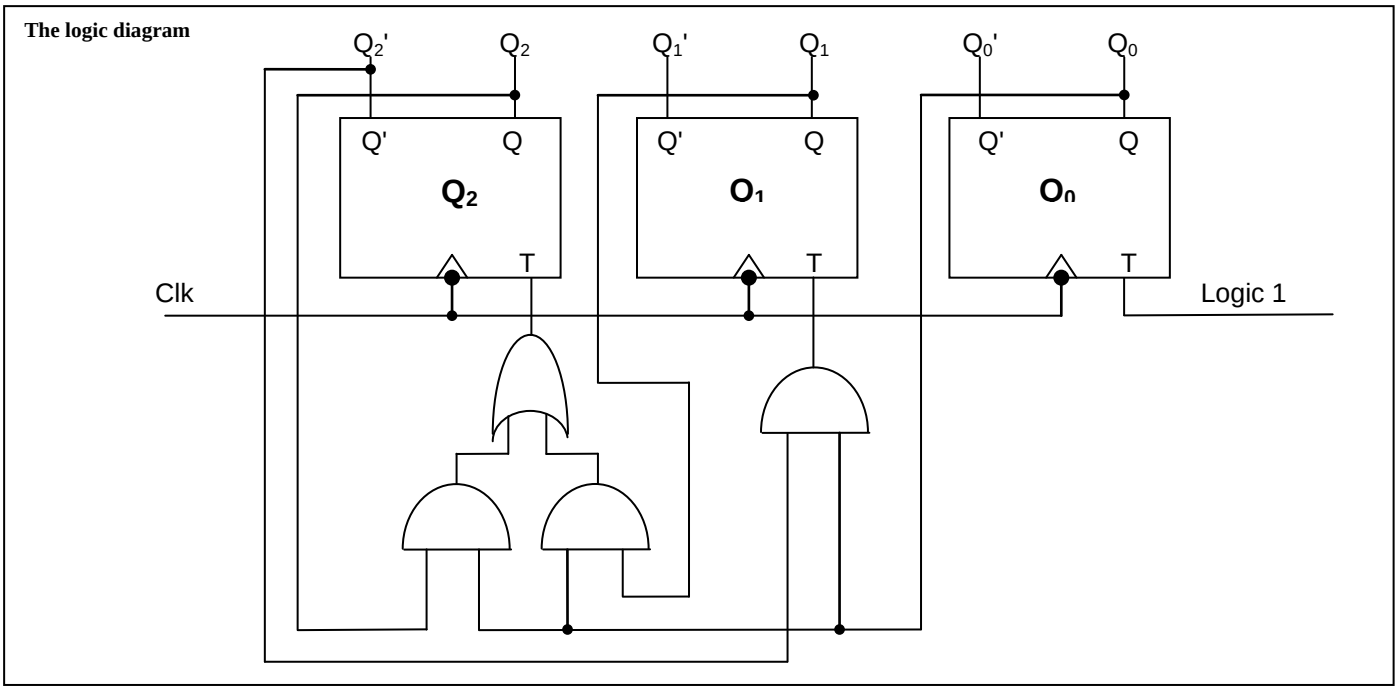
Present State			Next State			Flip-Flop Inputs		
Q2	Q1	Q0	Q2	Q1	Q0	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

$T0 = 1$

$T1 = Q_2' Q_0$

$T2 = Q_2 Q_0 + Q_1 Q_0$

The logic diagram



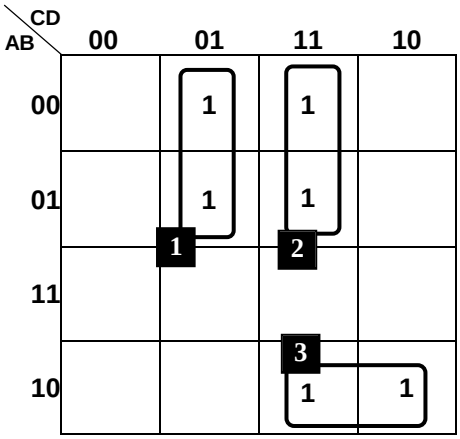
Question # 9: (8 Points)

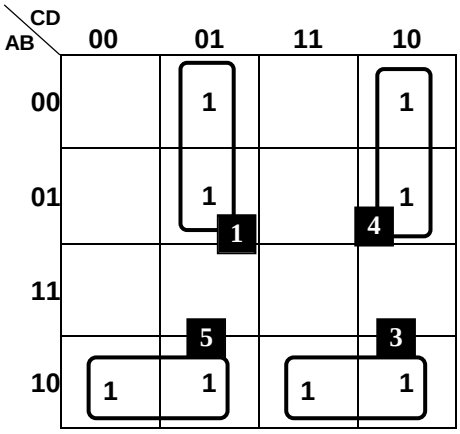
List the PLA programming table that implements the following Boolean functions using the minimum number of product terms:

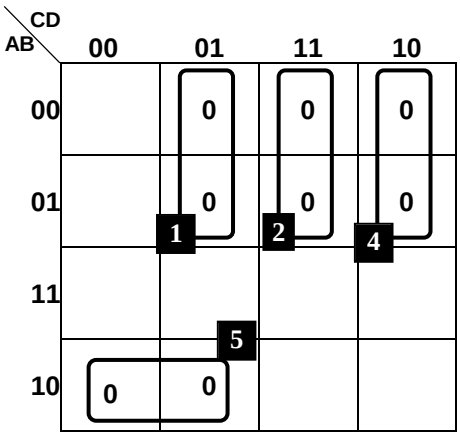
F1(A, B, C, D) = Σ m(1, 3, 5, 7, 10, 11)

F2(A, B, C, D) = Σ m(1, 2, 5, 6, 8, 9, 10, 11)

F3(A, B, C, D) = Σ m(0, 4, 10, 11, 12, 13, 14, 15)







PLA Programming Table

Product Term	Inputs				Outputs		
	A	B	C	D	(T) F1	(T) F2	(C) F3
1: A'C'D	0	-	0	1	1	1	1
2: A'CD	0	-	1	1	1	-	1
3: AB'C	1	0	1	-	1	1	-
4: A'CD'	0	-	1	0	-	1	1
5: AB'C'	1	0	0	-	-	1	1

F1 = A'C'D + A'CD + AB'C

F2 = A'C'D + AB'C + A'CD' + AB'C'

F3' = A'C'D + A'CD + A'CD' + AB'C'

****** Best Wishes ******

Prof. Magdy M. Doss