Assiut University
Faculty of Engineering

EE0513-ELECTRONIC CIRCUITS
First Term Final Exam
January 2016

Mechatronics Program

Attempt all questions, full mark: 40 Points **Time: 3 Hours**

Question #1: (10 Points)
Mark True (✓) or False (x)

X	1)	The dc load line intersects the horizontal axis of a transistor characteristic curve at $V_{CE} = V_{CC}/2$.
✓	2)	Base bias is less stable than voltage-divider bias.
✓	3)	The ***r*** parameter β_{ac} is the same as the ***h*** parameter h_{fe}
✓	4)	In a CE amplifier, the gain can be stabilized by using a swamping resistor.
X	5)	A bypass capacitor in a ***CE*** amplifier decreases the voltage gain.
✓	6)	A differential amplifier amplifies the difference of two input signals.
✓	7)	Each transistor in a class B amplifier conducts for half of the entire input cycle.
✓	8)	Class ***AB*** operation overcomes the problem of crossover distortion.
✓	9)	Darlington transistors can be used to increase the input resistance of a class AB amplifier.
X	10)	The channel resistance of a JFET is a constant.
X	11)	Forward transconductance of a JFET is the change in drain voltage for a given change in gate voltage.
X	12)	The JFET drain current I_D becomes zero at the pinch-off voltage.
X	13)	There is no phase inversion in a CS amplifier using JFET.
✓	14)	A CS amplifier using a D-MOSFET can operate with both positive and negative input voltages.
X	15)	CMOS is a device used in linear amplifiers.
✓	16)	An analog switch is controlled by a digital input.
X	17)	An ideal op-amp has very high output impedance.
X	18)	The closed-loop voltage gain of the op-amp inverting amplifier is dependent on the internal open-loop voltage gain of the op-amp.
✓	19)	A comparator with hyteresis has two trigger points.
X	20)	When a triangular waveform is applied to a differentiator, a sine wave appears on the output.

Question #2: (6 Points)
Choose the right answer:

1) A transistor circuit has V_{CC} = 12 V, V_{BB} = 8 V, R_C = 4 KΩ, R_B = 50 KΩ, and β_{DC} = 80, the transistor is

A
(A) being driven into saturation (B) being driven into cutoff
(C) being driven in the active region (D) operating nonlinearly

2) The β_{DC} of a transistor is its

B
(A) voltage gain (B) current gain
(C) power gain (D) internal resistance

3) The input resistance of a common-base amplifier is

A
(A) very low (B) very high
(C) the same as a CE (D) the same as a CC

4) An amplifier that operates in the linear region at all times is

A
(A) Class A (B) Class AB
(C) Class B (D) Class C

5) The efficiency of a power amplifier is the ratio of the power delivered to the load to

C
(A) the input signal power (B) the power dissipated in the last stage
(C) the power from the dc power supply (D) none of these answers

6) The peak current a class A power amplifier can deliver to a load depends on the

B
(A) maximum rating of the power supply (B) quiescent current
(C) current in the bias resistors (D) size of the heat sink

7) In a JFET, I_{DSS} is

C
(A) the drain current with the source shorted (B) the drain current at cutoff
(C) the maximum possible drain current (D) the midpoint drain current

8) The channel of a JFET is between the

B
(A) gate and drain (B) drain and source
(C) gate and source (D) input and output

9) For a p-channel JFET, drain current in the constant-current region increases when

A
(A) the gate-to-source bias voltage decreases (B) the gate-to-source bias voltage increases
(C) the drain-to-source voltage increases (D) the drain-to-source voltage decreases

10) A MOSFET differs from a JFET mainly because

C
(A) of the power rating (B) the MOSFET has two gates
(C) the JFET has a pn junction (D) MOSFETs do not have a physical channel

11) The op-amp common-mode gain is

B
(A) very high (B) very low
(C) always unity (D) unpredictable

12) When you apply a triangular waveform to the input of a differentiator, the output is

C
(A) a dc level (B) an inverted triangular waveform
(C) a square waveform (D) a sinusoidal waveform

Question #3: (10 Points)

a) If a transistor has a ***dc*** beta of 190, V_B = 2 V, and I_E = 4 mA, what is the ***dc*** input resistance at the base?

$R_{in(Base)}$ = 95 KΩ

b) Explain swamping.

Partially bypassing the emitter resistance to improve amplifier gain stability and increase its input impedance.

c) What characteristic of the common-collector amplifier makes it a useful circuit?

It has high input impedance.

d) What is the main advantage of the class-B amplifier over the class-A one?

It has greater efficiency.

e) An n-channel E-MOSFET has $I_{D(on)}$ = 8 mA at V_{GS} = 3 V, and $V_{GS(th)}$ = 2.5 V. Find I_D when V_{GS} = 4 V.

K = 32 mA/V^2
I_D = 72 mA

f) In a certain self-biased n-channel JFET circuit, I_D =8 mA and R_S = 1 KΩ. Determine V_{GS}.

V_{GS} = -8 V

g) If the gate-to-source voltage in an n-channel D-MOSFET is made more negative, what would be the effect on the drain current?

Decreases.

h) What is the major difference in construction of the D-MOSFET and the E-MOSFET?

D-MOSFET has a built in channel.

i) Define the op-amp common-mode rejection.

It is the ability of an op-amp to produce very low common mode gain compared to the differential mod gain.

j) What is the feedback element in an ideal op-amp diffrentiator?

Resistance.

Question #4: (2 Points)

The silicon ***npn*** transistor used in the common-collector amplifier shown in Fig.4 has $\beta_{dc} = \beta_{ac} = 120$.

a) Find r_e'.
b) Draw the ac equivalent circuit of the amplifier
c) Find the exact voltage gain and the total input impedance of the amplifier.

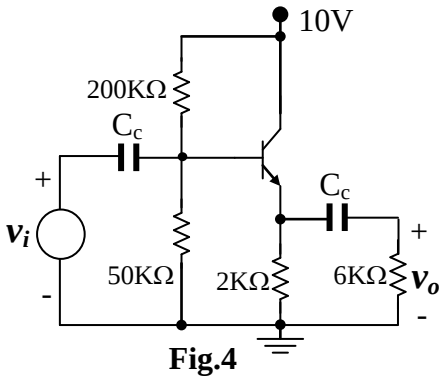


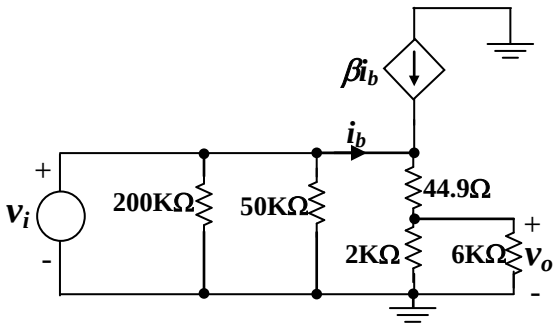
Fig.4

r_e'= 44.9 Ω

A_v= 0.97

Z_{in}= 32.9 KΩ

The ac equivalent circuit



Question #5 (3 Points)

The silicon ***npn*** transistor used in the swamped class-***A*** power amplifier of Fig.5 has $\beta_{dc} = \beta_{ac} = 100$. The collector resistor serves also as the load resistor. The input is a sinusoidal voltage with a 1V p-p, Determine:

a) The dc Q-point (I_{CQ} and V_{CEQ}).
b) The voltage gain A_v.
c) The signal power in the load P_L.
d) The total power from the power supply P_{DC}.
e) The amplifier efficiency η.

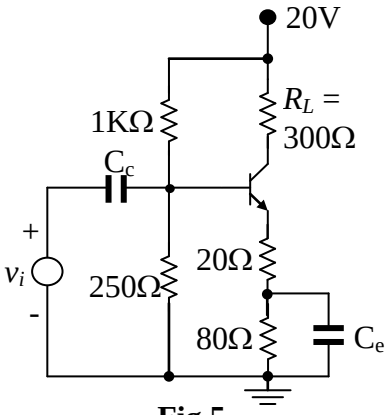


Fig.5

I_{CQ} = 32.35 mA

V_{CEQ} = 7.06 V

A_v = -14.44

P_L = 87 mW

P_{DC} = 647 mW

η = 13.45%

Question #6: (2 Points)

The JFET used in the common source amplifier of Fig.6 has $V_{GS(off)}$ = -4V and I_{DSS} = 12 mA.

a) Find R_S to set up a midpoint bias.
b) Determine the drain-source voltage V_{DS} at the Q- point.
c) Calculate the value of the transconductance g_m at the Q-point.
d) Determine the amplifier voltage gain.

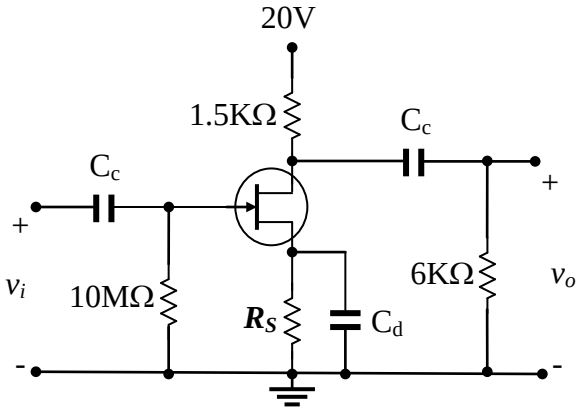


Fig.6

R_S= 196 Ω	V_{DSQ}= 9.82 V
g_m= 4.24 mS	A_v= -5.1

Question #7: (3 Points)

The E-MOSFET used in the common-source amplifier in Fig.7 has $I_{D(on)}$ = 135 mA at V_{GS} = 4 V and $V_{GS(th)}$ = 2.5 V.

a) Determine the operating point V_{GSQ}, I_{DQ} and V_{DSQ}.
b) Calculate the value of the transconductance g_m at the Q-point.
c) Determine the voltage gain and input impedance of the amplifier.

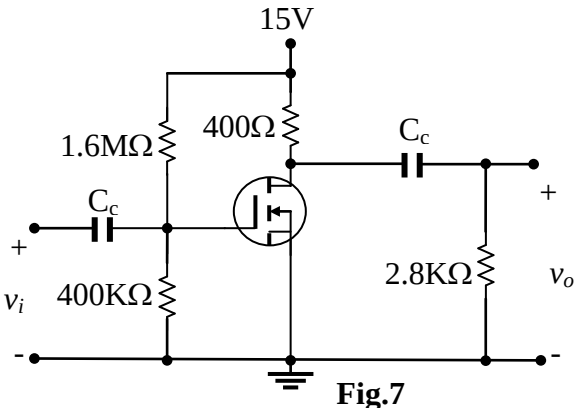


Fig.7

V_{GSQ}= 3V	I_{DQ}= 15 mA	V_{DSQ} = 9 V
g_m= 60 mS	A_v= -21	Z_{in}= 320 KΩ

Question #8 (2 Points)

Write the necessary nodal equations then find the voltages v_1 and v_o in the circuit of Fig.8, assuming ideal op-amp.

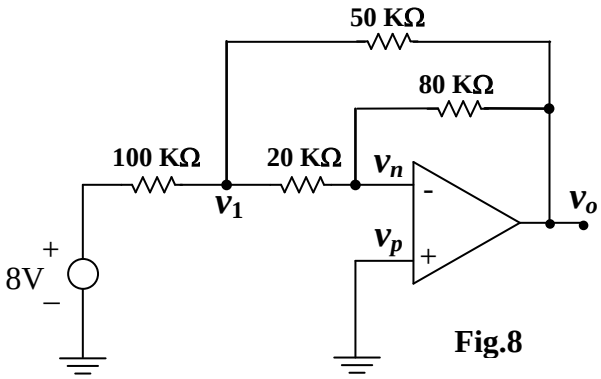


Fig.8

$4\,v_1 - v_o = 4$

$4\,v_1 + v_o = 0$

$v_1 = 0.5$ V

$v_o = -2$ V

Question #9: (2 Points)

a) Find an expression for the output voltage $v_o(t)$ of the integrating amplifier of Fig.9.
b) If a step voltage of -4 V is applied to the input, with no energy stored in the capacitor. Sketch $v_o(t)$ for $t \geq 0$.
c) How many milliseconds (T) elapse before the op-amp saturates?

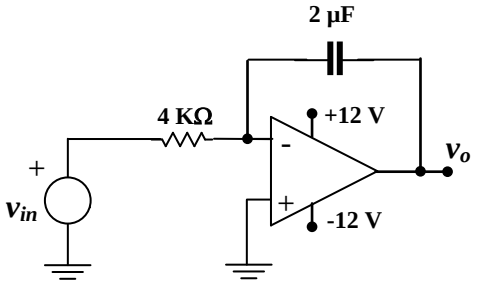
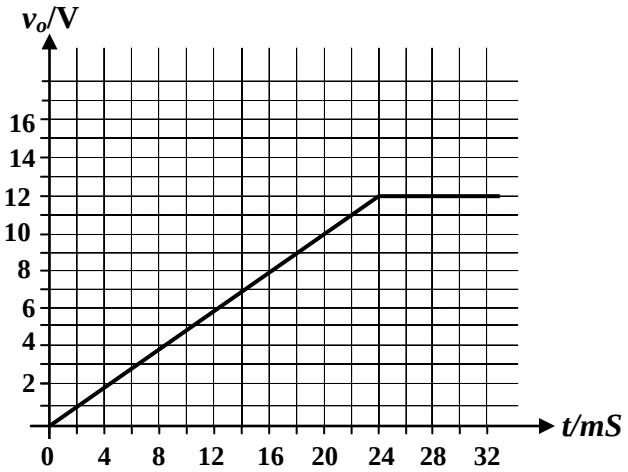


Fig.9

$$v_o(t) = -125 \int v_{in} dt + K$$

$T = 24$ mS



********** Best Wishes **********

Prof. Magdy M. Doss